LOW NOISE, LOW POWER SENSOR INTERFACE CIRCUITS FOR SPECTROSCOPY IN STANDARD CMOS TECHNOLOGY OPERATING AT 4 K

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ABSTRACT

In the framework of the Photodetector Array Camera and Spectrometer (PACS) project (for the European Herschel Space Observatory) IMEC designed the Cold Readout Electronics (CRE) for the Ge:Ga far-infrared detector array. Key Specifications for this circuit were high linearity (3%), very low power consumption (80µW for an 18 channel array), and very low noise (200 e^-) at an operating temperature of 4.2K (LHT- Liquid Helium Temperature). We have implemented this circuit in a standard CMOS technology (AMIS 0.7µm), which guarantees high production yield and uniformity, relatively easy availability of the technology and portability of the design. However, the drawback of this approach is the anomalous behavior of CMOS transistors at temperatures below 30-40K, known as kink and hysteresis effects and under certain conditions the presence of excess noise. These cryogenic phenomena disturb the normal functionality of commonly used circuits or building blocks. We were able to overcome these problems and developed a library of digital and analog building blocks based on the modeling of cryogenic behavior, and on adapted design and layout techniques. These techniques have been validated in an automated cryogenic test set-up developed at our institute. We will present here in detail the full design of the 18 channel CRE circuit, its interface with the Ge:Ga sensor, and its electrical performance and demonstrate that all major specifications at 4.2 K were met. We will equally present the techniques used to integrate and validate the circuit for its use at these extremely low temperatures.
Other designs and topologies for low noise and low power will be equally presented.

1. INTRODUCTION.

The Photoconductor Array Camera and Spectrometer (PACS)[1,2] is one of the three scientific instruments aboard the Herschel Space Observatory (HSO, formerly called FIRST)[3], ESA's fourth cornerstone mission in the Horizon 2000 program[4]. PACS makes use of two Ge:Ga photoconductor arrays (25 x 16 pixels), simultaneously imaging the band from 60 - 210 µm. In this band background limited performance is expected, with sensitivities around 2.5 10^{-18} W/m^2. The optimized photo-detector array design, requiring an operating temperature as low as 1.2 K, is developed to achieve high quantum efficiency and therefore high signal-to-

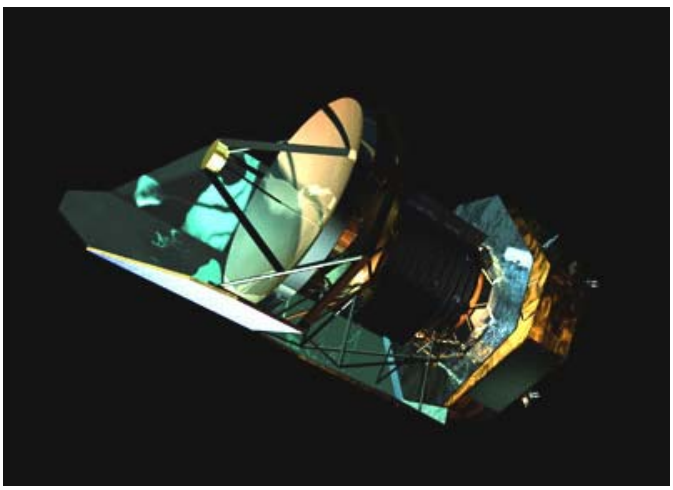

Figure 1 : Artist's impression of Herschel. The image shows telescope, vessel containing the liquid helium cryostat (narrow, middle part) and service module at the bottom.

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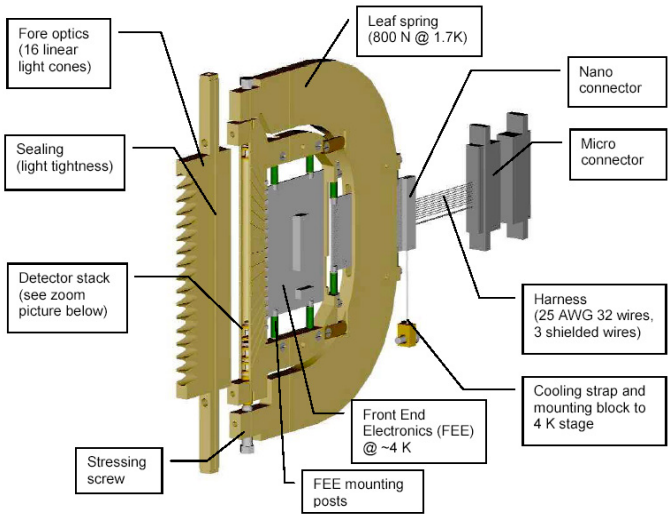

Figure 2 : Integrated detector module ; 1 element of the Ge:Ga array showing the optics, detector elements and the CRE integrated in the Front End Electronics (FEE) as shown.

noise ratios, so that observation times are minimized[5,6]. Some effort has been undertaken to match the performance of these detectors to the electrical performance of the Read Out Integrated Circuit (ROIC), operating at 4.2 K. IMEC has studied in detail the performance of CMOS transistors at Liquid Helium Temperature (LHT), which lead to the development of a new type of Cold Readout Electronics (CRE). The quality of the analog read-out electronics is critical for the overall performance of the integrated hybrid sensor. At higher temperatures, i.e. temperatures above the temperature where freeze-out occurs, analog design methods are very well known and documented, allowing the designer to optimize circuit and layout for a certain type of detector. However, this is not the case at lower temperatures, i.e. below 30K, where, although the behavior of individual MOS transistors has been studied in detail, there exist virtually no guideline nor design rule for the design of building blocks that will operate satisfactorily.

The readout circuit that will be presented in this paper is a Capacitive Feedback TransImpedance Amplifier (CTIA) circuit. It consists of 18 (16 + 2 dummy) so called channels - i.e. current integrators with an output buffer and the associated digital circuitry for the multiplexer. To avoid self-heating, the power dissipation of the CRE (power consumption for each amplifier had to be less than 5μW for a supply voltage of 5.5V). To ensure stable biasing of the detectors, the open loop gain of the integrating amplifier had to be higher than 1000 (60dB). Furthermore, the multiplexer unit had to be able to clock the integrated voltages at 20KHz speed, provide a linearity better than 3 %, and generate very low noise (200 e").

2. CIRCUIT DESIGN AT LHT AND BASIC BUILDING BLOCKS.

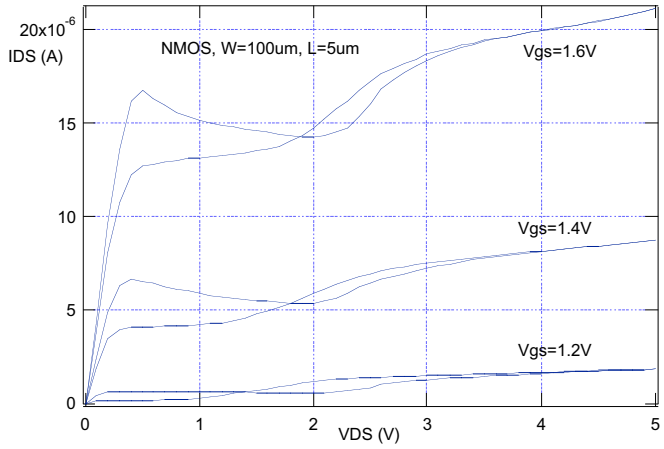

Figure 3 : I_{DS} in a NMOS transistor as a function of V_{DS} for various Gate Source voltages at 4.2 K. Kink and hysteresis effects are clearly visible.

IMEC selected for this circuit a standard CMOS technology (AMIS, n-well, mixed analog/digital, 0.7 µm), which guaranteed high production yield and uniformity, relatively easy availability of the technology and portability of the design. However, the drawback of this approach is the anomalous behavior of CMOS transistors at temperatures below 30-40K, known as kink and hysteresis effects and under certain conditions the presence of excess noise. Figure 3 shows the I_{DS} versus V_{DS} curves for an n-channel MOS transistor (V_{DS} swept from 0 to 5V). One can see that the curves exhibit the kink effect. As the drain-source voltage exceeds some critical voltage (about 2 V), impact ionisation around the drain generates minority carriers that are swept from the drain to the source[7]. Because of the freeze-out, the impedance of the substrate is very high and the carriers accumulate under the gate of the transistor, causing a drop in its threshold voltage and hence, an increase of its drain current[8]. The value of the technological gains Kn and Kp were extracted from the $\sqrt{I_{DS}}$ versus V_{GS} curves. We noticed that the technological gain is multiplied by as much as five for both n-channel and p-channel transistors. This is in agreement with earlier publications reporting mobilities of 1000 cm^2/Vs at 300K and 5000 cm^2/Vs at 4.2K in other CMOS processes[9,10]. The observed hysteresis, which is very pronounced for n-channel transistors below 30 K has been explained with the various mechanisms of conduction and recombination[11,12].

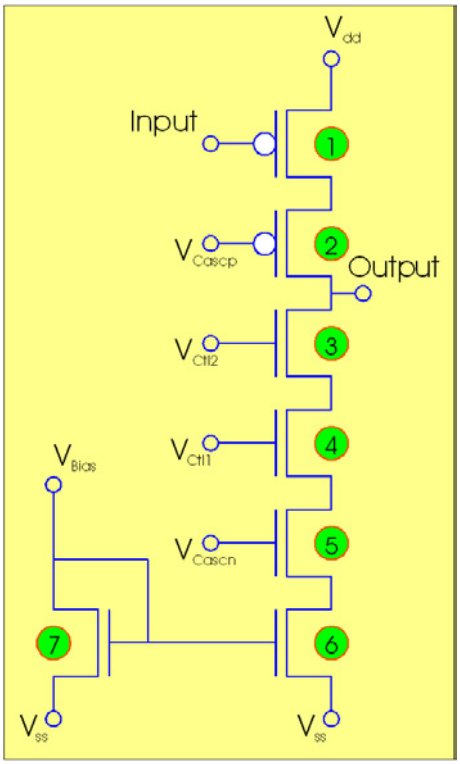

Figure 4 : Core amplifier schematic. The schematic is based on a cascode amplifier with added transistors for bias and hysteresis control. The measured voltage gain was over 8000 (78 dB).

Threshold voltage variations can be overcome using cascode structures[13,14], similar to those used in SOI technologies to solve the floating body effect. Whenever buffer amplifiers are necessary, p-type buffers are preferred since these transistors do not exhibit pronounced kink behaviour. To avoid entering into the kink region of n-type transistors, the reference voltages of the cascode

transistors are fixed in such a way that the drain to source voltage of any n-type transistor can never exceed 2 V.

The heart of the integrating amplifier was therefore chosen to be a cascode structure with added transistors for bias and hysteresis control (Figure 4). Transistor 7 will bias the circuit through transistor 6, and the two cascode transistors (5 and 2) will boost the gain with at least two orders of magnitude. Gains as high as 78 dB (8000) at 4 K have been reported. Transistors 3 and 4 limit the V_{DS} voltage of the n-type transistors, as explained before, so that transistors 3, 4, 5 and 6 will never enter the kink region., and never exhibit excess cryo noise. The amplifiers equilibrium voltage equals ~ 3.5 V for a supply voltage V_{DD} of 5 V.

Operation of CMOS logic circuits and switches pose no problem at LHT[15]. Kink and hysteresis are of no importance for switching, nor are noise considerations. Since the change of threshold voltage for p-type and n-type devices are opposite, the operation of a logical gate does not suffer from this effect. Dynamic CMOS logic will also show no problem, as the gate storage times become very long at 4.2 K. This will make the design of the digital driving electronics for the analog multiplexer very straightforward. Figure 5 shows, as an example, the integration capacitor selection circuit. The circuit allows the

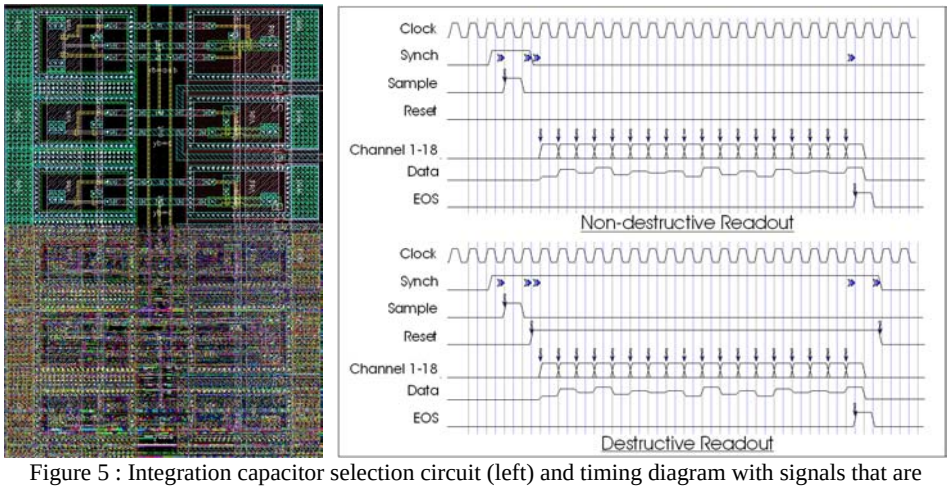

Figure 5 : Integration capacitor selection circuit (left) and timing diagram with signals that are provided to the chip (Synch and Clock), and signals that are generated on-chip (Reset, Sample, Data transfer and End-Of-Scan)(right). The digital selection circuit allows the selection of 4 integration capacitors with two signal lines.

selection of 4 integration capacitors with two signal lines. The driving signals that are provided to the analog multiplexer are equally shown. As can be noticed, destructive (with integration capacitor recharge), and non-destructive readout (without reset) can be provided. The SYNCH signal, together with the CLOCK generates the start of a readout cycle, starting with a sample signal for the whole array, and the sequential readout of all the cells. At the end of the cycle, an EOS (End-Of-Scan) signal is generated. This signal can be used to trigger devices or arrays that are wired in series, so that different modules can be read out in a single effort. The analog multiplexer basically consists of a shift register that drives the switches to sequentially direct each cell's output to the output stage. It is important to provide enough substrate and well contacts (for n and p type transistors) to avoid so-called soft latch-up (caused by the presence of substrate currents).

The shift register will consequently be realized with standard logic based on the use of JK-type flip-flops

3. INTEGRATING AMPLIFIER, BUFFERS AND OUTPUT AMPLIFIER

The high gain cascode, discussed in the previous section was used as the core amplifier for a Capacitive feedback Trans Impedance Amplifier (CTIA). The CTIA circuit provides excellent bias control, which is required to provide nearly constant detector bias. The circuit requires normally a differential amplifier, but as in this case, it can be realized with a single ended amplifier that is AC coupled to the rest of the circuit. The AC coupling will at the same time recalibrate the amplifier such that drift and offset, as well as hysteresis effects at low temperatures will not degrade the amplifier performance.
The full schematic of the AC coupled CTIA circuit, as proposed by IMEC can be found

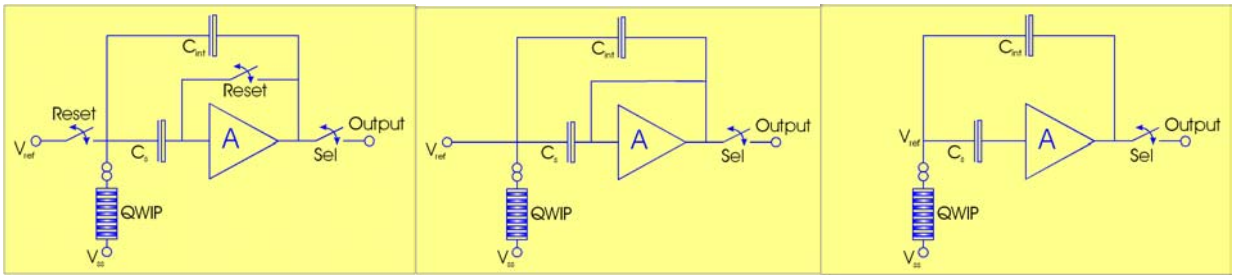

Figure 6 : AC coupled integrating amplifier (left). During reset, the input is connected to a reference and the amplifier is shorted (middle). During integration, the circuit behaves like a CTIA (right).

in Figure 6. During reset, the amplifier is configured in feedback, so that its output and input voltage are identical. The input node (the detector node) is at the same time fixed to a reference voltage (used as a detector bias node). During this phase, the feedback capacitor C_{int} as well as the AC couple capacitor C_s will be charged to a voltage equal to V_{ref} minus the amplifiers equilibrium voltage. This phase is comparable to a full reset of the integrator.
After the reset, during integration, the circuit behaves as a traditional CTIA circuit. The amplifier, together with the couple capacitance acts as a single ended amplifier, and will fix the bias point variation of the detector during integration:

$$\Delta V_{ref} = \frac{I_{\det} \cdot t}{(1+A) \cdot C_f}$$

With I_{det} the detector current. This variation should be less then 1 mV (requirement), which results in a high (at least 10^3) amplifier gain A. The integrators output voltage is given by:

$$\Delta V_{out} = -\frac{A}{1+A} \cdot \frac{I_{\det} \cdot t}{C_f} \approx -\frac{I_{\det} \cdot t}{C_f}$$

The complete Flight Model (FM) channel schematic is shown in figure 7. A DC offset voltage stored over a leveling capacitor was used to shift the DC levels into the dynamic range of the two buffers.

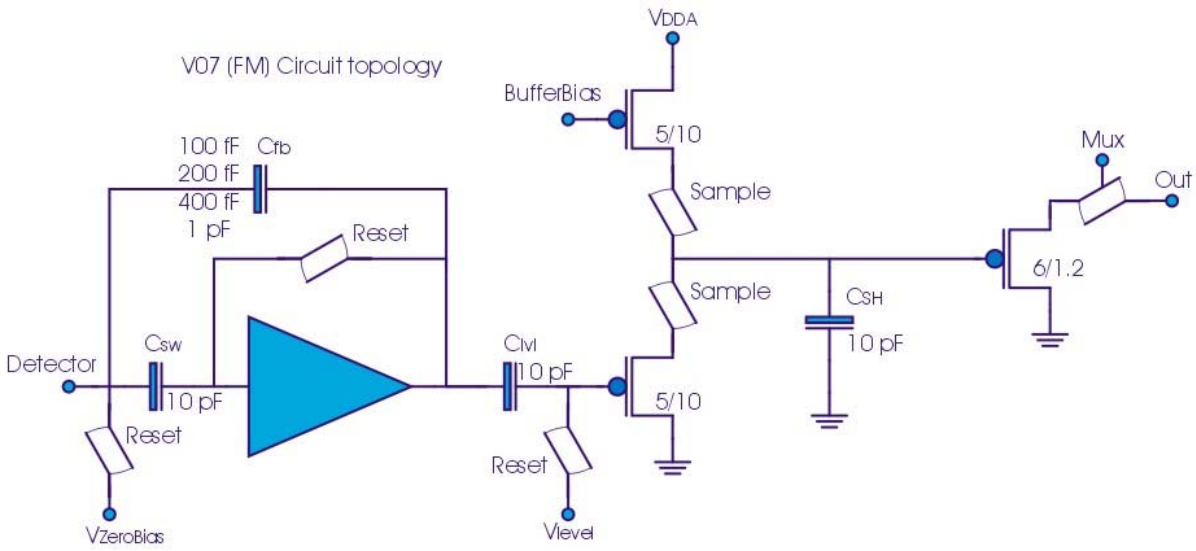

Figure 7 : Complete CRE channel. The channel consists of an integrating amplifier, followed by a level capacitor to shift the DC loutput levels of the integrator into the dynamic range of the source followers, a S/H buffer stage and an output amplifier.

4. INTEGRATION AND QUALIFICATION

This included the verification of the compatibility of the bond material with 4 K operation, optimization of the bond-yield and temperature cycling (between room-temperature and LHT) of the devices. Other tests on qualification models would focus on cryogenic vibration (figure 8) tests to demonstrate launch survivability and exhaustive temperature cycling to qualify the assembly procedure.

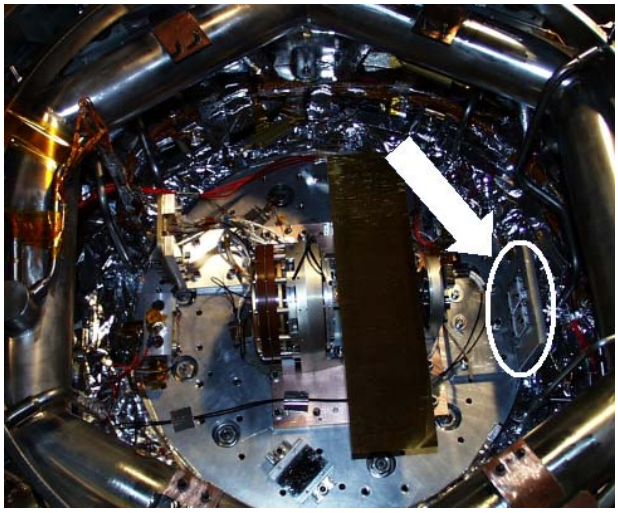

Figure 8 : 2 PACS qualification models in a cryogenic shaker.

An important step in the validation of the assembly procedure is the verification of the bonding (interconnect) and the mounting (mechanical stability) of the passives. This has been performed during cryocyling tests. This test consisted in subsequent heating and cooldown of samples with mounted and bonded passives. At the start of the test (reference), and after each of two series of 25 cycles, destructive (2 g) and non-destructive pull and shear tests were performed, and their results analyzed. The tests revealed no significant influence of the cycling neither on bond quality nor on the quality of fixation of the passives. Figure 10 gives an overview of the bond quality for the different types of bonds that were tested

(substrate-substrate and substrate-passive). On the average, we measured a destructive pull-force of 11 and 7 g. The spread was very low (the average pull strength was higher than 7 times the spread) indicating high reliability. The shear force required to remove a passive was between 5 and 8 kg for a capacitor, and 0.7 and 0.8 kg for a resistor.

The cryogenic vibration tests have been performed at CSL (Centre Spaciale de Liège) and revealed no problems.

Several tests have been introduced in the production cycle of the flight models to guarantee high reliability of the assembled modules. After wafer production, dies are screened and only those with optimal performance selected. After assembly, all substrates are visually inspected to verify bond (wire and wire fixation) and mounting (glue). This step is then followed by three cryocycles to identify weaknesses in the assembly process, and exhaustive electrical performance testing at 4 K.

The actual production yield is higher that 75 %. The 25 % loss includes devices that are functional exhibiting one ore more channels with 30-40 % higher noise than the others. Non-functional devices or devices with bad ("dead") channels after assembly are very rare and have until now not been identified.

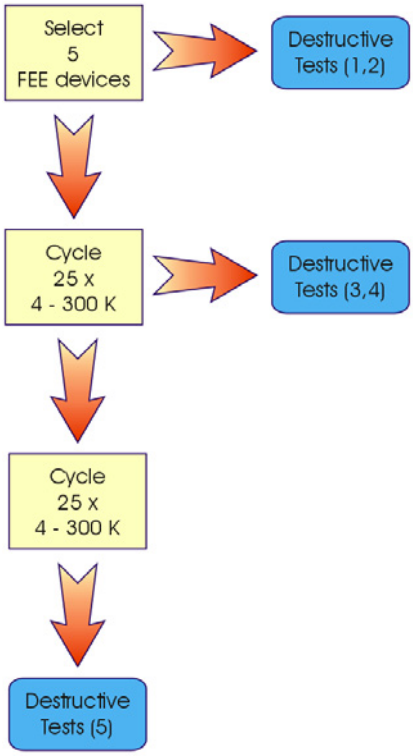

Figure 9 : Device flow during cryocycling tests.

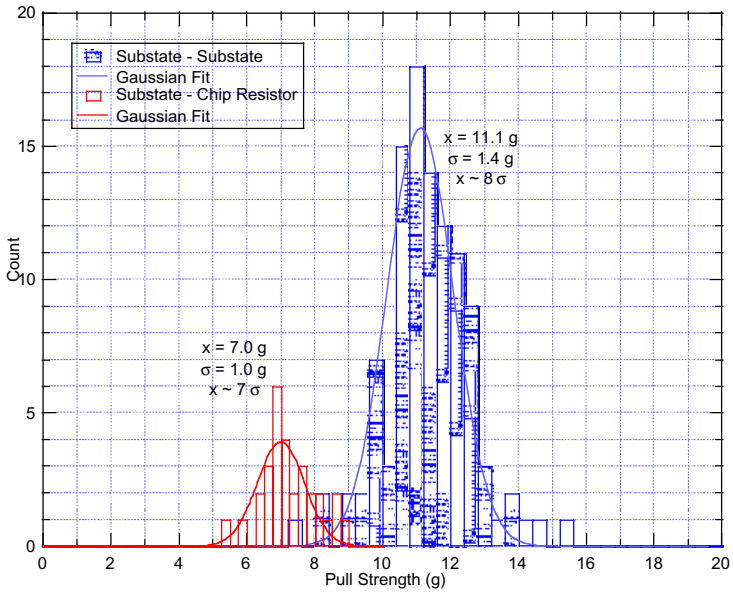

Figure 10 : Overview of bond quality (destructive pull-test results) for 2 types of bonds. Average pull strength was 7 or 11 g with a spred that was small enough to assure good reliability.

5. MEASUREMENTS

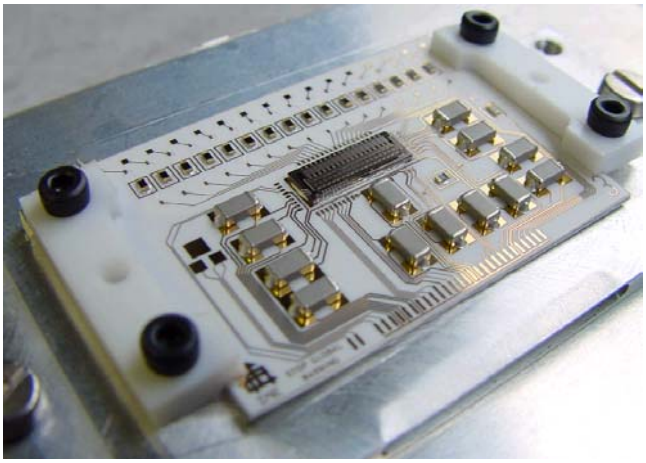

Figure 11 : Photograph showing the 18 channel CRE chip mounted on a ceramic substrate ; substrate dimensions are 36 x 26 mm.

The circuit presented in the previous sections was mounted on a ceramic substrate, which also contained passive elements used to provide stable bias currents to the circuit. Die selection confirmed the high process yield of a standard CMOS process. A photograph of the CRE circuit mounted on the substrate is shown in figure 10. The power supply voltage V_{DD} was set to 5.5 V. During noise measurements, a battery set was used to provide all analog voltages. The clock frequency was set to 8.3 kHz. The circuit's power dissipation was equal to 74 µW (this figure does not include the dissipation of the output amplifier fed by an off-chip current source). The output dynamic range was found to be higher than 2 V for all selected integration capacitors (100 fF, 200 fF, 400 fF and 1 pF).

We measured the integrating amplifiers linearity, input referred noise and the noise of the 18 CRE channels, from input to output with the multiplexer operating at the aforementioned frequency. During the noise measurements, all input channels were left open (unconnected). The results were very satisfactory. The non-linearity over the whole output dynamic range of the integrator was better than 2 % for all implemented values of the integration capacitor (this value includes the non-linearities of the analog multiplexer and the S/H circuitry). A typical graph with integration slope and its deviation from a linear fit is shown in Figure 12.

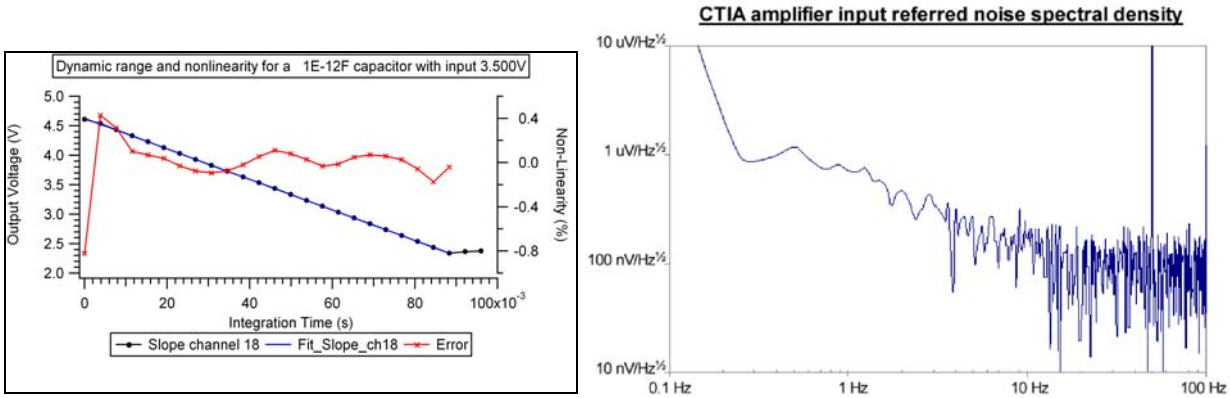

Figure 12 : Typical output slope of one channel (left) and input referred noise spectral density of the integrating amplifier (right). The Non-Linearity is here better than 0.8 %. For all selectable capacitors Non-Linearity was better than 2 % over the whole dynamic range (more than 2V).

The noise measurements on a single cascode amplifier (input referred noise spectral density - Figure 11) were according to the specifications (lower than 1 μV/√Hz @ 1 Hz and 100 nV/√Hz @ 30 Hz). Measurements on a complete array, mounted on a ceramic substrate, indicated an average current noise (referred to the input of the circuit) of 2.29 10^{-17} A/√Hz or 405 noise electrons. Uniformity over the whole array was around 20 %.

Channel #	*Current Noise (A/√Hz)*	*Noise electrons*
1	2.16 10^{-17}	381
2	2.57 10^{-17}	454
3	2.25 10^{-17}	397
4	3.57 10^{-17}	630
5	1.93 10^{-17}	341
6	2.63 10^{-17}	465
7	2.19 10^{-17}	386
8	2.24 10^{-17}	396
9	1.70 10^{-17}	300
10	1.69 10^{-17}	298
11	2.09 10^{-17}	369
12	1.69 10^{-17}	298
13	2.90 10^{-17}	512
14	2.51 10^{-17}	444
15	1.78 10^{-17}	314
16	2.41 10^{-17}	425
17	2.16 10^{-17}	382
18	2.78 10^{-17}	490

Table 1 : Current noise and number of noise electrons for the 18 different channels of a typical CRE device.

6. CONCLUSIONS AND FUTURE WORK

The proposed design approach performs according to the majority if its specifications, and shows that the advantages of a standard CMOS process (high yield, low cost and good reproducibility) are compatible with cryogenic circuit design. Power dissipation and linearity are according to specifications, but the measurements indicate a noise performance somewhat higher than specified but still compatible with the performance of the detector arrays.

Future work will consist in further improvement of the noise performance. Since

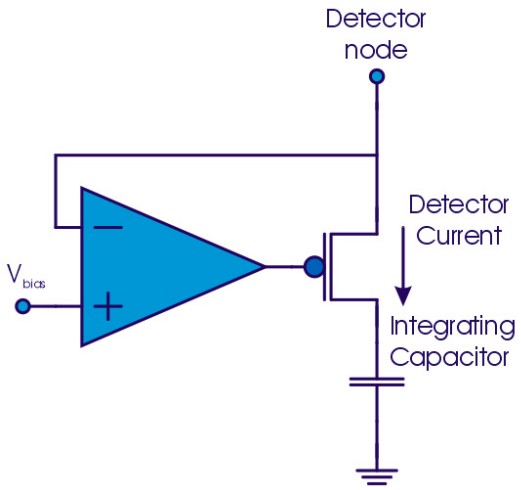

Figure 13 : Feedback Enhanced Direct Injection topology. Future design based on this topology will allow improvement of noise performance.

a large part of the noise is injected through the substrate, improved substrate contacting can provide a solution. Reduction of the parasitic input capacitor and a change in topology can further improve noise performance (figure 13).
The present circuit will served as a basis for ESA's DARWIN mission. In the framework of this project, our team developed a cryogenic 180 channel, 30µm pitch, Readout Integrated Circuit (ROIC) for flip-chip integration (figure 14).
The presented cascode core amplifier will allow the design of fast AC coupled comparator circuits that will lead to AD converters for use at cryogenic temperatures. The transmission of analog data between detector and data collection unit can be quite cumbersome on a satellite, since high signal quality or large bandwidth and low noise over a relatively long distance (often different meters of cable) requires high power. Data conversion in the readout stage can provide a solution. The transmission of binary data is far less noise sensitive, and less demanding than that of analog data.

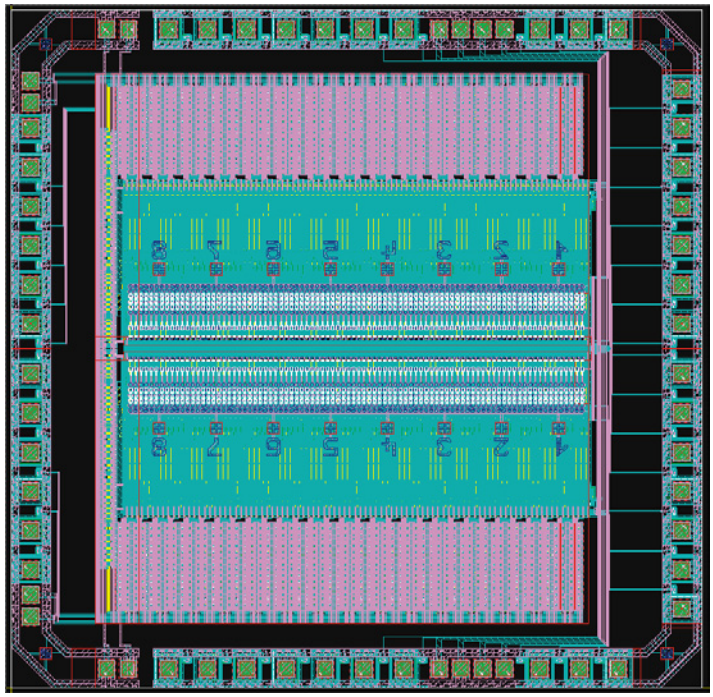

Figure 14 : 180 channel, 30µm pitch, Readout Integrated Circuit (ROIC) for flip-chip integration used for Darwin.

7. ACKNOWLEDGEMENT

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REFERENCES

[1] A.Poglitsch, C.Waelkens, and N.Geis in IR Spaceborn Remote Sensing, Proc. SPIE 3759,p. 221,1999
[2] A.Poglitsch, An optimized photoconductor instrument for FIRST, A.Wilson ed. ESA SP-401,p.25,1997
[3] G.Pilbratt, The FIRST mission : Baseline, science objectives and operations, ESA SP-401, p.7,1997
[4] Space Science-Horizon 2000, ESA SP-1070,1984
[5] S.Kraft, O.Frenzl,L.Hermans,R.Katterloher,D.Rosenthal,U.Groezinger, J.W.Beeman in IR Spaceborn Remote Sensing VII, Proc SPIE 3759, p.214,1999

[6] S.Kraft, O.Frenzl,O.Charlier,T.Cronje,R.Katterloher,D.Rosenthal,U.Groezinger, J.W.Beeman, UV, Optical and IR Space telescopes and Instruments, Proc SPIE 4013, 2000, p.233
[7] Shoji Anamura, Masaaki Aoki, Toshiaki Masuhara, Osamu Minato, Yoshio Sakai and Testsuya Hayashida, Operation of Bulk CMOS Devices at Very Low Temperatures, IEEE Journal of Solid State Circuits, Vol. SC-21, NO.3, pp. 484-489 June 1986.
[8] K.J. McCall, Mosfet Characteristics at 4.2K, Ext. Abstracts of the El. Chem.Soc fall meeting, pp.491-492.
[9] Kamgar, Subthreshold Behavior of Silicon MOSFET's at 4.2K, Solid State Electronics, Vol. 25, pp.537-539, 1982.
[10] Roy L.Maddox, p-MOSFET Parameters at Cryogenic Temperatures, IEEE Transactions on Electron Devices, Vol.23, pp. 16-21, 1976.
[11] B. Dierickx, L. Warmerdam, E.Simoen, J.Vermeiren and C.Claeys, Model for Hysteresis and Kink Behavior of MOS Transistors Operating at 4.2K, IEEE Transaction on Electron Devices, Vol. 35, pp. 1120-1125, 1988.
[12] E. Simoen, B. Dierickx and C. Claeys, Analytical Model for the Kink in nMOST's operating at liquid Helium Temperatures (LHT), Solid State Electronics, Vol. 33, pp.445- 454, 1990.
[13] W. Redman-White, R. Lucas, R. Dunn, and P. Smithers, A radiationhard AGC stabilized SOS crystal oscillator, IEEE J. Solid-State Circuits,vol. 25, pp. 282-288, Feb. 1990.
[14] W. Redman-White, B. M. Tenbroek, M. S. L. Lee, C. F. Edwards, M. J.Uren, and R. J. T. Bunyan, Analogue design issues for SOI CMOS, in Proc. 1996 IEEE Int. SOI Conf., Oct. 1996, pp. 6-8.
[15] M.J.Deen, Cryogenic operation of CMOS-based microsystems and computers, Microprocessors & systems, vol 13-4, pp.245-253, 1989.